Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-16 (canceled).

Claim 17 (currently amended): A method for time synchronization of a switching computer system having at least one main computer with, in each case, at least one assigned secondary computer, each main and secondary computer being respectively provided with at least one internal clock and being connected via at least one ATM bus, the method comprising the steps of:

transmitting, via the at least one main computer and along the ATM bus, with an N-th interrupt of a sequence of interrupts which are transmitted at a fixed time interval, a synchronization message with a time indication ~~and, if appropriate, a time stamp~~, the time indication corresponding to a time of day of the main computer at an instant of the N-th interrupt plus the fixed time interval;

reading, via the at least one secondary computer ~~and with good probability~~, the synchronization message via the ATM bus;

setting, via the at least one secondary computer, the internal clock of the at least one secondary computer to the communicated time indication upon the occurrence of ~~the~~ next interrupt;

transmitting, via the at least one secondary computer and along the ATM bus, a success message with an identifier of the secondary computer to the main computer;

reading, via the main computer, the success message;

deciding, via the main computer, based on a message propagation time, whether the success message was transmitted at a proper time;

defining, in the case of a correctly timed transmission, the corresponding secondary computer as synchronized; and

defining, in the case of a non-correctly timed transmission, the corresponding secondary computer as unsynchronized.

Claim 18 (previously presented): A method for time synchronization of a switching computer system as claimed in claim 17, wherein, between the interrupts of the sequence of interrupts, further interrupts can occur which are not taken into account in the time synchronization method.

Claim 19 (previously presented): A method for time synchronization of a switching computer system as claimed in claim 17, wherein the main computer, with the (N + 2)-th interrupt, again performs the time synchronization method.

Claim 20 (previously presented): A method for time synchronization of a switching computer system as claimed in claim 17, wherein a specific secondary computer is defined as synchronized if the success message arrives at the main computer between the (N + 1)-th and the (N + 2)-th interrupt.

Claim 21 (previously presented): A method for time synchronization of a switching computer system as claimed in claim 17, wherein the time interval is 23.5 msec.

Claim 22 (previously presented): A method for time synchronization of a switching computer system as claimed in claim 17, wherein the switching computer system includes further main computers which, in turn, have a superordinate computer at least with regard to system time, the further main computers being synchronized with one another as with the main and secondary computers.

Claim 23 (previously presented): A method for time synchronization of a switching computer system as claimed in claim 17, wherein the communicated time indication also contains a date.

Claim 24 (previously presented): A method for time synchronization of a switching computer system as claimed in claim 17, wherein the ATM bus is an AMX bus.

Claim 25 (currently amended): A switching computer system, comprising:

at least one main computer having at least one internal clock;

at least one secondary computer having at least one internal clock, the at least one secondary computer being assigned to the ~~with~~ at least one main computer;

at least one ATM bus connecting the at least one main and the at least one secondary computers;

~~when~~ wherein the at least one main computer transmits, with an N-th interrupt of a sequence of interrupts which are transmitted at a fixed time interval, via the ATM bus, a synchronization message with a time indication ~~and, if appropriate, a time stamp~~, the time indication corresponding to a time of day of the main computer at the instant of the N-th interrupt plus the fixed time interval;

wherein the at least one secondary computer reads the synchronization message via the ATM bus, its respective internal clock being set to the communicated time indication upon ~~the~~ occurrence of a next interrupt of the sequence, and transmits a success message with an identifier of the secondary computer to the main computer via the ATM bus;

wherein the main computer reads the success message and decides, based on a message propagation time, whether the success message was transmitted at a proper time;

wherein, in the case of a correctly timed transmission, a definition of the corresponding secondary computer as synchronized is stored in a memory of the main computer; and

~~and~~ wherein, in the case of a non-correctly timed transmission, a definition of the corresponding secondary computer as unsynchronized is stored in the memory.

Claim 26 (previously presented): A switching computer system as claimed in claim 25, wherein between the interrupts of the sequence of interrupts, further interrupts can occur which are not taken into account in time synchronization.

Claim 27 (previously presented): A switching computer system as claimed in claim 25, wherein the main computer includes a repetition part which, with the (N+2)-th interrupt, again performs time synchronization.

Claim 28 (previously presented): A switching computer system as claimed in claim 25, wherein the main computer defines a specific secondary computer as synchronized if the success message arrives at the main computer between the (N+1)-th and the (N+2)-th interrupt.

Claim 29 (previously presented): A switching computer system as claimed in claim 25, wherein the fixed time interval is 23.5 msec.

Claim 30 (previously presented): A switching computer system as claimed in claim 25, further comprising:

further main computers which, in turn, have a superordinate computer at least with regard to system time, the further main computers being synchronized with one another as with the main and secondary computers.

Claim 31 (previously presented): A switching computer system as claimed in claim 25, wherein the communicated time indication also contains a date.

Claim 32 (previously presented): A switching computer system as claimed in claim 25, wherein the ATM bus is an AMX bus.